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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,723	01/03/2002	Gregory C. Desalvo	AFD 459	2134

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,723	DESALVO ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,22-25 and 27-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,22-25 and 27-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claim 26 in paper filed on 01/12/2004.

2. Claims 1-9, 22-25 and 27-37 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 9, 31-34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayama et al. (U.S. 6,440,822 B1) in view of Morcom et al. (U.S. 6,162,702).

In reference to claims 1, 3, 31, 33, 34 and 37, Hayama et al. (Figs.1A-1E) in a related method to form MMIC teach forming an array of via holes (2) of selected location and depth dimension in a wafer of circuit die (1); said via holes (2) being formed after forming said MMIC and located in response to selected microwave radio frequency electrical component locations over said front side surface of said wafer of circuit die (1); said step of forming an array of via holes (2) being performed during a front side accessing of said wafer of circuit die (1); forming a layer of metal conductor (3) on said array of via holes (2); removing a layer of selected thickness form a backside surface of said wafer (1), exposing backside portions of said formed front side via holes (2); and interconnecting front side and backside ground plane microwave radio frequency

energy conveying metal conductors (2) of said wafer circuit die by way of metallic conductors (9, 10) traversing said via holes (2) (column 4, line 24 – column 6, line 37).

Hayama et al. fail to teach disposing a grid pattern mask on said on the backside of a wafer comprising silicon; said grid pattern mask including a backside periphery outline masking for each circuit die of said wafer; and removing a layer of selected thickness form said wafer backside surface, wherein said removing being from exposed backside surface areas intermediate elements of said grid pattern masking, wherein said removing step leaving recessed valley portions of selected thickness disposed intermediate individual circuit die-strengthening upstanding surrounding bluff masked semiconductor regions in said wafer backside surface. However, Morcom et al. (1A-6) in a related method to form ultra thin silicon wafers for power devices teach disposing a grid pattern (4, 5) on the backside of a silicon wafer (2) comprising silicon; said grid pattern mask (4, 5) including a backside periphery outline masking for each circuit die of said wafer (2); and removing a layer (1) of selected thickness form said wafer backside surface, wherein said removing being from exposed backside surface areas intermediate elements of said grid pattern masking (4, 5), wherein said removing step leaving recessed valley portions of selected thickness disposed intermediate individual circuit die-strengthening upstanding (3) surrounding bluff masked semiconductor regions in said wafer backside surface (column 2, line 15 – column 3, line 45). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hayama et al. and Morcom et al. to enable the removing step of Hayama et al. to be performed according to the teachings of Morcom et al. for the further advantage of

providing mechanical support for the wafer during the removing process (Morcom et al., column 1, lines 34 – 48) and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed removing step of Hayama et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 2, the combined teachings of Hayama et al. and Morcom et al. substantially teach all aspects of the invention but fail to disclose wherein said wafer has an initial overall thickness between five hundred and six hundred twenty five micrometers and has a final thickness of between twenty five and one hundred micrometers in said removed layer recessed valley portions. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed.

Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claim 4, the combined teachings of Hayama et al. and Morcom et al. substantially teach all aspects of the invention by fail to show forming an etching step vernier marker pattern in each die backside surface of said wafer after said step of forming an array of front side via hole. However, portion of the ridges in Morcom et al. (see Fig.6) could perform the function required of by recitation of "vernier markers", which is a label or statement of intended use.

In reference to claim 5, the combined teachings of Hayama et al. and Morcom et al. teach wherein said backside periphery outline masking is disposed in a closed geometric pattern encircling each front side microwave radio frequency circuit die and further include a closed geometric backside annular ring of original wafer thickness semiconductor material surrounding said entire wafer of microwave radio frequency circuit die (Morcom et al., column 2, line 53 – column 3, line 6).

In reference to claims 6 and 7, the combined teachings of Hayama et al. and Morcom et al. teach wherein said step of removing selected thickness from said wafer backside surface etching step comprises a backside etching sequence (Morcom et al., column 2, lines 23 – 33); wherein said backside surface etching step comprises a dry gas etching step (Morcom et al., column 2, lines 23 – 33).

In reference to claim 9, the combined teachings of Hayama et al. and Morcom et al. teach wherein said removing step individual circuit die-strengthening upstanding

surrounding bluff masked regions further include a wafer periphery-surrounding annular ring upstanding bluff region (Morcom et al., Fig.6).

In reference to claim 32, the combined teachings of Hayama et al. and Morcom et al. teach wherein said array of circuit die locations and circuit die segregation boundaries defined across a frontal surface of said semiconductor wafer and said upstanding mesa array of original wafer thickness extent across said backside surface each comprise a rectangular grid pattern (Morcom et al., Fig.6).

5. Claims 8 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Hayama et al. ('822) in view of Morcom et al. ('702) as applied to claims 1-7, 9, 31-34 and 37 above, and further in view of Kohno et al. (U.S. 6,358,762 B1).

The combined teachings of Hayama et al. and Morcom et al. teach wherein said backside etching step includes dry etching (Morcom et al., column 2, lines 22 – 32), but fail to teach wherein said dry etching includes inductively coupled plasma. However, Kohno et al. (Figs.4A-4F) in a related method to etch semiconductor substrates teach etching said semiconductor substrate (11) using inductively coupled plasma (column 3, lines 44 – 50, column 6, lines 3 – 11 and column 9, lines 14 – 29). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hayama et al. and Morcom et al. with Kohno et al. to enable the etching step of Hayama et al. and Morcom et al. to be performed according to the teachings of Kohno et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching

step of Hayama et al. and Morcom et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

6. Claims 22-26, 28, 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayama et al. ('822 B1) in view of Morcom et al. ('702) and Yamada et al. (U.S. 6,297,131 B1).

In reference to claims 22, 26, 30 and 36, Hayama et al. (Figs.1A-1E) in a related method to form MMIC teach forming an array of via holes (2) of selected location and depth dimension in a wafer of circuit die (1); said via holes (2) being formed after forming said MMIC and located in response to selected microwave radio frequency electrical component locations over said front side surface of said wafer of circuit die (1); said step of forming an array of via holes (2) being performed during a front side accessing of said wafer of circuit die (1); forming a layer of metal conductor (3) on said array of via holes (2); removing a layer of selected thickness form a backside surface of said wafer (1), exposing backside portions of said formed front side via holes (2); interconnecting front side and backside ground plane microwave radio frequency energy conveying metal conductors (2) of said wafer circuit die by way of metallic conductors (9, 10) traversing said via holes (2); and separating each circuit die (column 4, line 24 – column 6, line 37).

Hayama et al. fail to teach disposing a grid pattern mask on said on the backside of a wafer comprising silicon; said grid pattern mask including a backside periphery outline masking for each circuit die of said wafer; and removing a layer of selected thickness form said wafer backside surface, wherein said removing being from exposed

backside surface areas intermediate elements of said grid pattern masking, wherein said removing step leaving recessed valley portions of selected thickness disposed intermediate individual circuit die-strengthening upstanding surrounding bluff masked semiconductor regions in said wafer backside surface. However, Morcom et al. (1A-6) in a related method to form ultra thin silicon wafers teach depositing a mask (4, 5) of grid pattern-defining configuration on wafer (2) backside surface; said mask (4, 5) of grid pattern-defining configuration determining a plurality of wafer (2) backside grid cells each aligned in surrounding periphery with one of said wafer (2) frontal surface integrated circuit devices; removing a controlled thickness (1) amount of semiconductor wafer (2) backside surface semiconductor material within each said backside grid cell, said removing including an etching step and leaving a wafer (2) backside grid pattern of semiconductor material of said semiconductor wafer (2) nominal thickness dimension and leaving a selected thickness remainder amount of said semiconductor wafer (2) nominal thickness dimension material, within each said backside grid cell, supporting said integrated circuit device; said etching step also leaving a wafer perimeter-disposed backside ring (3) of wafer semiconductor material of said semiconductor wafer (2) nominal thickness dimension and integral interconnection with said wafer backside grid pattern of wafer nominal thickness dimension; said wafer perimeter-disposed backside ring of wafer semiconductor material of said semiconductor wafer nominal thickness dimension and said wafer backside grid pattern of wafer nominal thickness dimension semiconductor material in interconnecting combination adding physical handling-assisting substantial physical integrity and rigidity to said now thinned semiconductor

wafer (column 2, line 15 – column 3, line 45). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hayama et al. and Morcom et al. to enable the removing step of Hayama et al. to be performed according to the teachings of Morcom et al. for the further advantage of providing mechanical support for the wafer during the removing process (Morcom et al., column 1, lines 34 – 48) and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed removing step of Hayama et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Hayama et al. and Morcom et al. fail to teach further processing said wafer during continued frontal surface mounting, said further processing including separating each circuit die by removing said each integrated circuit device die from said wafer by wafer segregation within a lateral extent of a backside grid cell. However, Yamada et al. (Figs.1A-6) in a related method to form separated dies teach processing a wafer (30) during a continued frontal surface mounting, said further processing including removing each integrated circuit device die (30A) from said wafer (30) by wafer segregation within a lateral extent of a backside grid cell ([0040] – [0043]). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hayama et al. and Morcom et al. with the teachings of Yamada et al. to enable the separation step of Hayama et al. and Morcom et al. to be performed according to the teachings of Yamada et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative

suitable methods of performing the disclosed separation step of Hayama et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 23, the combined teachings of Hayama et al., Morcom et al. and Yamada et al. teach wherein said step of forming a plurality of via hole intrusions into said semiconductor wafer includes disposing said via hole intrusions to a first depth dimension into said semiconductor wafer; and wherein said selected thickness remainder amount of said semiconductor wafer nominal thickness dimension material in said step of removing a controlled thickness amount of said wafer backside semiconductor material within each said backside grid cell comprises leaving a selected thickness remainder amount of said wafer nominal thickness equal to said via, hole intrusions first depth dimension into said semiconductor wafer (Morcom et al., column 2, line 53 – column 3, line 6.

In reference to claim 24, the combined teachings of Hayama et al., Morcom et al. and Yamada et al. teach wherein said semiconductor wafer of nominal thickness is between five hundred and six hundred twenty-five micrometers in thickness; and wherein said selected thickness remainder amount of said wafer nominal thickness and said via hole intrusions first depth dimension are each no more than one hundred micrometers (Morcom et al., column 3, lines 7 – 18).

In reference to claim 25, the combined teachings of Hayama et al., Morcom et al. and Yamada teach wherein said circuit device is comprised of field effects transistors (Hayama et al., column 5, lines 33 – 42).

In reference to claim 28, the combined teachings of Hayama et al., Morcom et al. and Yamada et al. teach wherein said etching removing step comprises a dry gas etching step (Morcom et al., column 2, lines 23 – 33).

7. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayama et al. ('822 B1) in view of Morcom et al. ('702) and Yamada et al. ('131 B1) as applied to claims 22-26, 28, 30 and 36 above, and further in view of Matsunami (U.S. 5,463,246).

The combined teachings of Hayama et al., Morcom et al. and Yamada et al. substantially teach all aspects of the invention but fail to teach wherein said depositing step mask is a metallic mask. However, Matsunami (Figs.2a-2d) in a related method to form field effect transistors teaches etching a semiconductor substrate (1) using a metallic mask (6) (column 6, lines 7 – 50). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hayama et al., Morcom et al. and Yamada et al. with Matsunami to enable the depositing step mask step of Hayama et al., Morcom et al. and Yamada et al. to be performed according to the teachings of Matsunami because osk would have been motivated to look to alternative suitable methods of performing the disclosed depositing step mask step of Hayama et al., Morcom et al. and Yamada et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morcom et al. ('702) in view of Goldstein ('080) and Yamada et al. ('131 B1) as applied to claims 22-26, 28, 30 and 36 above, and further in view of Kohno et al. ('762 B1).

The combined teachings of Hayama et al., Morcom et al. and Yamada teach wherein said backside etching step includes dry etching, but fail to teach wherein said dry etching includes inductively coupled plasma. However, Kohno et al. (Figs.4A-4F) in a related method to etch semiconductor substrates teach etching said semiconductor substrate (11) using inductively coupled plasma (column 3, lines 44 – 50, column 6, lines 3 – 11 and column 9, lines 14 – 29). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hayama et al., Morcom et al. and Yamada with Kohno et al. to enable the etching step of Hayama et al., Morcom et al. and Yamada to be performed according to the teachings of Kohno et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Hayama et al., Morcom et al. and Yamada and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

9. Applicant's arguments with respect to claims 1-9, 22-25 and 27-37 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is 571-272-2800. See MPEP 203.08.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

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George Fourson
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